User's Guide

Publication Number E2467-97002
January 1997

For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2467A Intel APIC Bus Preprocessor Interface

The HP E2467A Preprocessor Interface—At a Glance

The HP E2467A Preprocessor Interface provides an APIC Bus interface for state analysis between any Intel APIC Bus target system and an HP logic analyzer. The HP E2467A can be used with the HP E2457A Preprocessor Interface to provide state, timing, and APIC analysis of an Intel Pentium® target system, or it can be used with the HP E2466A/B Preprocessor Interface to provide state, timing, and APIC analysis of an Intel Pentium® Pro target system. The following logic analyzers are supported for the listed configurations.

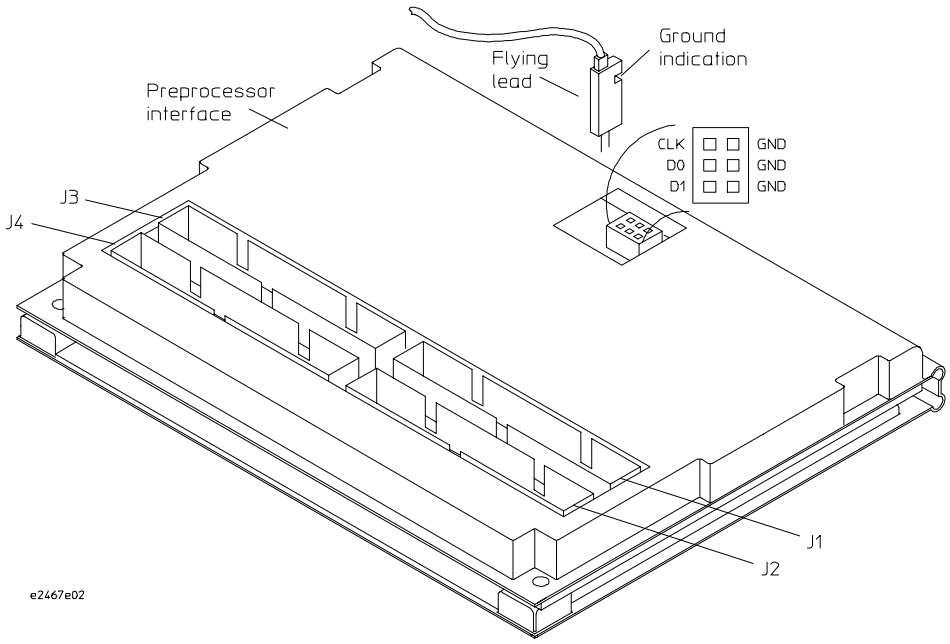
Logic Analyzers Supported

	APIC Analysis Only	APIC and Pentium®	APIC and Pentium® Pro
HP 16550A*	one card	two cards	two cards
HP 16554A*	one card	three cards	three cards
HP 16555A*	one card	three cards	three cards
HP 16556A*	one card	three cards	three cards

*Requires HP 16500B Mainframe with software version v3.04 or higher

The preprocessor interface provides the physical connection between the target system and the logic analyzer. The configuration software on the flexible disk sets up the logic analyzer for compatibility with the preprocessor interface.

For more information on the supported logic analyzers, microprocessors, or other preprocessor interfaces, refer to the appropriate reference manuals for those products.



HP E2467A Preprocessor Interface Assembly

In This Book

This book is the user's guide for the HP E2467A Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the APIC bus.

This user's guide is organized into three chapters:

Chapter 1 explains how to attach the preprocessor to the target system and how to configure the logic analyzer for analysis.

Chapter 2 provides reference information on the format specification and symbols configured by the preprocessor interface software and information about the inverse assembler and status encoding.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

Table of Contents

1 Setting Up the Preprocessor Interface

Equipment Configurations 1–3

Equipment Supplied 1–3
Minimum Equipment Required 1–4
Standalone APIC Interface 1–4
APIC Interface with HP E2457A Pentium® Preprocessor Interface for State and Timing Analysis of Pentium® 1–4
APIC Interface with HP E2466B Preprocessor Interface for State and Timing Analysis of Pentium® Pro 1–5

Connecting to the target system 1–6

To power up or power down 1–6
To connect the APIC preprocessor for standalone APIC Bus analysis 1–7
To connect to the target system through the Pentium® or Pentium® Pro preprocessor interface 1–9

Connecting to the Logic Analyzer 1–11

To connect to the HP 16550A analyzer 1–12
To connect to the HP 16554A/55A/56A analyzers 1–13

Loading the Preprocessor Interface Software 1-14

To load the configuration and inverse assembler into the HP 16500B mainframe 1–14

2 Analyzing the APIC Bus

Displaying Information 2–3

To display the format specification 2–3
To display the configuration symbols 2–5
To display captured state data 2–12

Using the Inverse Assembler 2–13

Inverse Assembler Exception Messages 2–15

Protocol violations 2–15

Triggering Hints 2–16

To capture actual APIC Bus serial line signals 2–17
To trigger on Delivery Mode 2–17
To trigger on a particular vector 2–17
To trigger on multiple criterion 2–18
To trigger on an APIC exception message 2–18
To trigger on Data in Remote Read message 2–18

3 Preprocessor Interface Hardware Reference

Operating Characteristics 3–3
Theory of Operation and Clocking 3–5
Signal-to-Connector Mapping 3–5
Circuit Board Dimensions 3–12
Repair Strategy 3–13

A If You Have a Problem

Analyzer Problems A–3

Intermittent data errors A–3
No activity on activity indicators A–4
No trace list display A–4

Preprocessor Problems A–5

Target system will not boot up A–5
Erratic trace measurements A–6
Capacitive loading A–6

Inverse Assembler Problems A–7

No inverse assembly or incorrect inverse assembly A–7
Inverse assembler will not load or run A–8

Intermodule Measurement Problems A–9

An event wasn't captured by one of the modules A–9

Messages A–10

". . . Inverse Assembler Not Found" A–10
"No Configuration File Loaded" A–10
"Selected File is Incompatible" A–10
"Measurement Initialization Error" A–11
"Slow or Missing Clock" A–12
"Time from Arm Greater Than 41.93 ms" A–12
"Waiting for Trigger" A–12

1

Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the HP E2467A Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers.

Equipment Configurations

This section lists the equipment supplied with the HP E2467A Preprocessor Interface, and the equipment required for the various measurement configurations. It also includes information about the logic analyzers supported by the HP E2467A.

Equipment Supplied

The HP E2467A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor circuit card.
- The HP 16500B inverse assembler software and configuration files on a 3.5-inch disk.
- The HP 16505A Prototype Analyzer inverse assembler software and configuration files, for use with the HP E2467A.
- Three flying leads, to attach the preprocessor interface to the target system. Included with the flying leads are four grabbers and three ground leads.
- This User's Guide.

Minimum Equipment Required

The HP E2467A Preprocessor Interface can be used in three different configurations: as a stand-alone APIC Bus interface, as an APIC interface with an HP E2457A Pentium® Preprocessor Interface, or as an APIC interface with an HP E2466A/B Pentium® Pro Preprocessor Interface. The part numbers and equipment are listed for each of these configurations.

Standalone APIC Interface

When used as an APIC interface, the preprocessor interface provides state analysis of the target system APIC bus. The following equipment is required for this configuration:

- The HP E2467A Preprocessor Interface, which includes the circuit card hardware and the configuration files and inverse assembler software.
- The flying leads. For some target systems, the grabbers are also required.
- An HP 16500B mainframe.
- One of the logic analyzers listed in the table at the end of this section.

APIC Interface with HP E2457A Pentium® Preprocessor Interface for State and Timing Analysis of Pentium®

When used with the HP E2457A preprocessor interface for state and timing analysis of Pentium® target systems, the following equipment is required:

- The HP E2467A Preprocessor Interface.
- The HP E2457A Preprocessor Interface hardware, which includes the combined configuration files and the inverse assembler software.
- The flying leads (grabbers not needed).
- An HP 16500B mainframe.
- One of the logic analyzers listed in the table at the end of this section.

APIC Interface with HP E2466B Preprocessor Interface for State and Timing Analysis of Pentium® Pro

When used with the HP E2466B Preprocessor Interface for state and timing analysis of Pentium® Pro target systems, the following is required:

- The HP E2467A Preprocessor Interface.
- The HP E2466B Preprocessor Interface hardware, which includes the combined configuration files and the inverse assembler software.
- The flying leads (grabbers not needed).
- An HP 16500B mainframe.
- One of the logic analyzers listed in the following table.

Logic Analyzer Characteristics

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16550A	102/card	100 MHz	250 MHz	4 k states
16554A	68/card	70 MHz	125 MHz	512 k states
16555A	68/card	110 MHz	250 MHz	1 M states
16556A	68/card	100 MHz	200 MHz	1 M states

Logic Analyzers Supported

Logic Analyzer	APIC Analysis Only	APIC and Pentium®	APIC and Pentium® Pro
HP 16550A*	one card	two cards	two cards
HP 16554A*	one card	three cards	three cards
HP 16555A*	one card	three cards	three cards
HP 16556A*	one card	three cards	three cards

*Requires HP 16500B Mainframe with software version v3.04 or higher

Connecting to the target system

Setting up the preprocessor interface hardware consists of the following major steps:

- Turn off power to the target system and the logic analyzer.
- If you are doing standalone APIC analysis, use the flying leads to connect the preprocessor interface to the target system.
- If you are using the APIC preprocessor interface with a Pentium® or Pentium® Pro preprocessor interface, connect the Pentium® or Pentium® Pro preprocessor interface to the target system, then use the flying leads to connect the APIC preprocessor interface to the Pentium® or Pentium® Pro preprocessor interface.

The following sections cover these topics in detail

To power up or power down

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

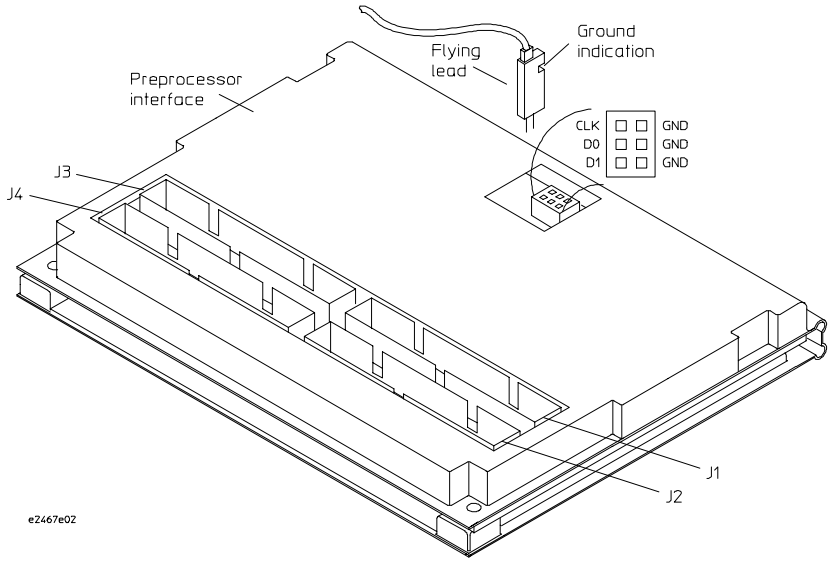
To connect the APIC preprocessor for standalone APIC Bus analysis

If you are performing only APIC Bus analysis, you must connect the APIC preprocessor interface directly to the APIC signals on the target system.

1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Connect the three flying leads to the six-pin APIC signal connector on the APIC preprocessor interface.

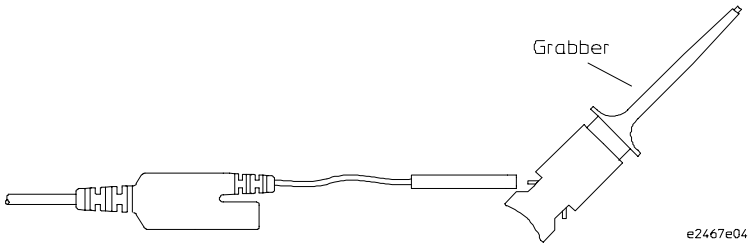
CAUTION

Ensure that you do not cross the signals and the grounds. The three active signals (CLK, D0, and D1) are located to the interior of the circuit board, and the three grounds are on the outside edge. The ground side of the flying lead connector has a notch (see below). Serious damage to the target system and/or the circuit board can result from improper connection.



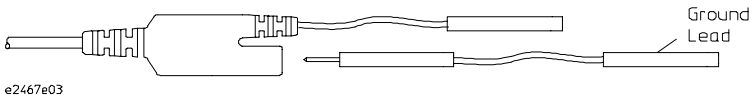
Connecting the Flying Leads to the APIC Connector

2 Locate the following signals on the target system: APIC Clk, D1, and D0. If necessary, use the grabbers to connect to each signal on the target system.



Optional Grabber

3 Connect a ground lead from one of the flying leads to an appropriate ground point on the target system. If necessary, use a grabber.



Ground Lead

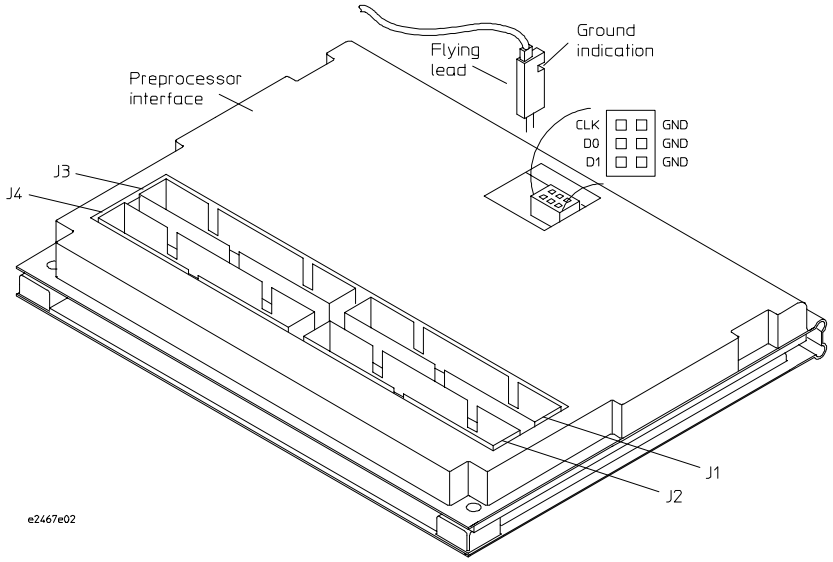
To connect to the target system through the Pentium® or Pentium® Pro preprocessor interface

If you are using the APIC bus preprocessor interface with the Pentium® or Pentium® Pro preprocessor interface, you can connect to the APIC signals through the Pentium® or Pentium® Pro preprocessor interface.

1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Use the directions in the Pentium® or Pentium® Pro User's Guide to connect the Pentium® or Pentium® Pro preprocessor interface to the target system.
3. Connect the three flying leads to the six-pin APIC signal connector on the APIC preprocessor interface.

CAUTION

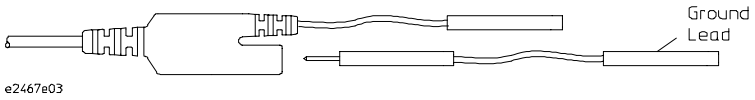
Ensure that you do not cross the signals and the grounds. The three active signals (CLK, D0, and D1) are located to the interior of the circuit board, and the three grounds are on the outside edge. The ground side of the flying lead connector has a notch. Serious damage to the target system and/or the circuit board can result from improper connection.



Connecting the Flying Leads to the APIC Connector

4 Locate the following signals on the Pentium® or Pentium® Pro preprocessor interface: APIC Clk, D1, and D0 (see illustration in appropriate User's Guide to find the headers where these signals are located). Use the flying leads to connect each signal to the appropriate pin on the the Pentium® or Pentium® Pro preprocessor interface.

5 Connect a ground lead from one of the flying leads to a ground pin on the Pentium® or Pentium® Pro preprocessor interface header.



Ground Lead

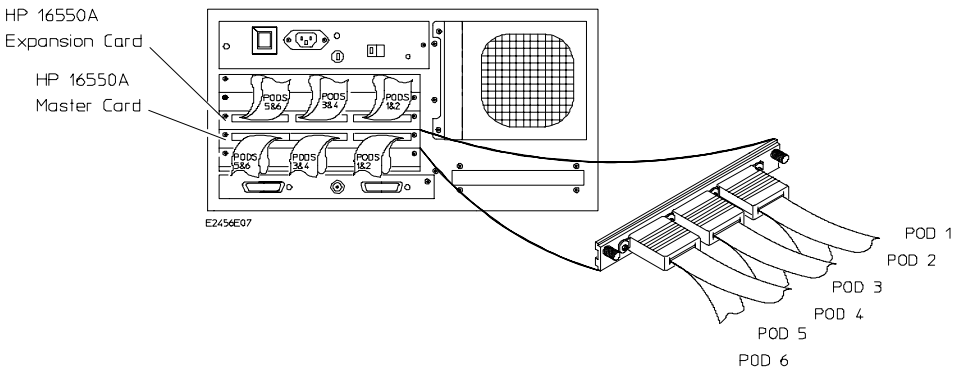
6 Refer to the user's guide that came with the Pentium® or Pentium® Pro for instructions on connecting the APIC Bus Preprocessor to the logic analyzer. Use the configuration files included with the Pentium® or Pentium® Pro preprocessor.

Connecting to the Logic Analyzer

The following sections show the connections between the logic analyzer pod cables and the connectors on the preprocessor interface. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

To connect to the HP 16550A analyzer

Use the table below to connect the preprocessor to the HP 16550A logic analyzer.



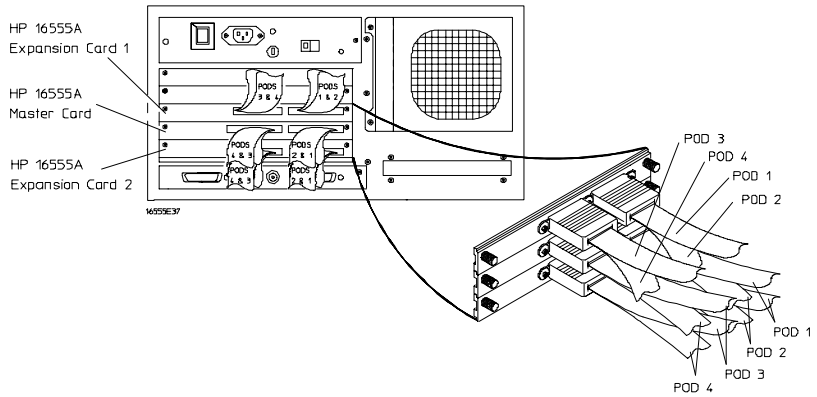
HP 16550A Expansion Card	Expansion Card Pod 6	Expansion Card Pod 5	Expansion Card Pod 4	Expansion Card Pod 3	Expansion Card Pod 2	Expansion Card Pod 1
HP E2467A Connector	not used	not used	not used	not used	not used	not used

HP 16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2467A Connector	not used	not used	J4 DATA_B	J3 DATA_B	J2 DATA	J1 DATA clk ↑

Configuration File
Use configuration file CAPICA01 if you are only using two pods with the HP 16550A logic analyzer, and CAPICA02 if you are using four pods with the HP 16550A logic analyzer. You must use the correct configuration file for the number of pods used, since the preprocessor interface auto detects the number of connected pods and adjusts accordingly.

To connect to the HP 16554A/55A/56A analyzers

Use the table below to connect the preprocessor to the HP 16554A/55A/56A.



HP 16554A/55A/56A Exp. Card 1	not used			
HP 16554A/55A/56A Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2467A Connector	J4 DATA_B	J3 DATA_B	J2 DATA	J1 DATA clk ↑
HP 16554A/55A/56A Exp. Card 2	not used			

Configuration File
Use configuration file CAPICA03 if you are only using two pods with the HP 16554A/55A/56A logic analyzer, and CAPICA04 if you are using four pods with the HP 16554A/55A/56A logic analyzer. You must use the correct configuration file for the number of pods used, since the preprocessor interface auto detects the number of connected pods and adjusts accordingly.

Loading the Preprocessor Interface Software

Configuring the logic analyzer consists of loading the software by inserting the floppy disk into the logic analyzer disk drive or HP 16505A Prototype Analyzer and loading the proper configuration file. The configuration file you use is determined by the logic analyzer you are using and whether or not you are using the HP 16505A Prototype Analyzer.

The HP 16505A Prototype Analyzer update disk provides HP 16505A-specific inverse assembler files and HP 16505A-specific configuration files. The HP 16505A configuration files assist in triggering on APIC messages. These configuration files are located in the /hp16505/config/apicbus directory, and have the same prefix names as the 16500B config files.

To load the configuration and inverse assembler into the HP 16500B mainframe

The first time you set up the preprocessor interface, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers with a hard disk, you might want to create a directory such as APIC on the hard drive and copy the contents of the "HP 16500B Logic Analyzer Configs" floppy onto the hard drive. You can then use the hard drive for loading files, instead of the floppy disk drives listed in step 2.

1. **Insert the "HP 16500B Logic Analyzer Configs" floppy disk in the front disk drive of the logic analyzer.**
2. **Go to the System Flexible Disk menu.**
3. **Configure the menu to load.**
4. **Use the knob to select the appropriate configuration file.**

   Choosing the correct configuration file depends on which analyzer you are using, and whether you are also using a Pentium® or Pentium® Pro preprocessor interface with the APIC preprocessor interface. The

configuration files are shown with the logic analyzer connection tables, and are also in the table below.

5 Select the appropriate analyzer (such as "100/500 MHz LA") for the load.

6 Execute the load operation on the menu to load the file into the logic analyzer.

The logic analyzer is configured for APIC analysis by loading the appropriate configuration file. Loading this file also automatically loads the correct inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	16500 Analyzer Description	Type of Analysis	Configuration File
16550A	100 MHZ STATE 500 MHZ TIMING	Two-pod APIC Four-pod APIC	CAPICA01 CAPICA02
16554A	0.5M SAMPLE 70/250 MHz LA	Two-pod APIC Four-pod APIC	CAPICA03 CAPICA04
16555A	1.0M SAMPLE 110/250 MHz LA		
16556A	1.0M SAMPLE 100/400 MHz LA		

APIC Configuration Files and Inverse Assembler

Analyzer Model	Type of Analysis	Configuration File	Inverse Assembler
16550A	Two-pod APIC Four-pod APIC	CAPICA01 CAPICA02	iapic2 iapic4
16554A/55A /56A	Two-pod APIC Four-pod APIC	CAPICA03 CAPICA04	iapic2 iapic4

2

Analyzing the APIC Bus

Analyzing the APIC Bus

This chapter describes how to display configuration information and preprocessor interface data, gives label and symbol encodings for the status field, and provides information about the inverse assembler.

Displaying Information

This section describes how to display logic analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

To display the format specification

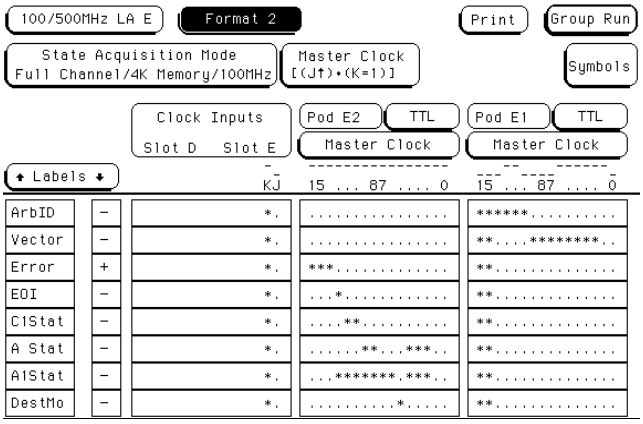
- **Select the format specification menu for your logic analyzer.**

  The APIC Bus configuration files contain predefined format specifications. These format specifications include all labels for monitoring the APIC bus.

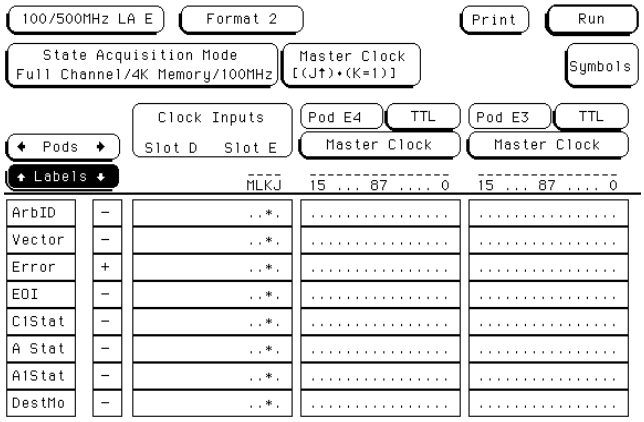
  Chapter 3 of this guide contains a table that lists the signals for the APIC Bus preprocessor and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the signals should be on the format specification screen.

Example

The format specification display shown in the following figure is from the HP 16550A logic analyzer. Additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.



Logic Analyzer Format Specification (two-pod logic analyzer)



Logic Analyzer Format Specification (four-pod logic analyzer)

To display the configuration symbols

- **Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.**

  The HP E2467A configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify APIC cycles. Labels simplify triggering on specific APIC Bus cycles. The label base in the symbols menu is set to hexadecimal to conserve space.

  The number of bits depends on the logic analyzer you are using. For some of the listings, a four-pod logic analyzer uses twice as many bits as a two-pod logic analyzer. A two-pod logic analyzer uses each pod twice for each cycle, therefore it only uses half as many logic analyzer bits.

  The first of the following tables describes the decode of the APIC Bus signals that are captured by the preprocessor. The second table lists the label and symbol encodings defined by the logic analyzer configuration software.

> Under the heading "Polarity", negative means that the logic analyzer inverts the signal. Positive means that the logic analyzer does not invert the signal.

Signal/Label List

Label Name	Polarity	Number of bits 2/4-pod	Description
APIC Message Signals			
ArbID	negative	7	Arbitration ID
Vector	negative	11	Interrupt Vector
Error	positive	6	Error number
EOI	negative	4	EOI Status
C1Stat	negative	5	Checksum
A Stat	negative	8	A status
A1Stat	negative	11	A1 status
DestMo	negative	5	Destination Mode
Delive	negative	7	Delivery mode
Level	negative	5	Level (physical or logical)
Trigge	negative	5	Trigger (edge or level)
Prior	negative	7	Priority Arbitration ID
TieID	negative	10/14	Lowest Priority Tie Arbitration ID
S Stat	negative	5/8	S status
C2Stat	negative	5/8	Remote Read Data checksum
A2Stat	negative	8/10	A2 status
DestID	negative	11/11	Destination ID
UData	negative	19/22	Upper 16 bits of data
LData	negative	19/22	Lower 16 bits of data
Buffered APIC Signals			
PICD1	positive		APIC D1
PICD0	positive		APIC D0
Inverse assembler symbols			
ADDR	positive	32	unused
DATA	negative	32	signals from pods 1 and 2
DATA_B	negative	32	signals from pods 3 and 4
STAT	positive	32	status signals from pods 1 and 2

The following table lists the label and symbol encodings defined by the logic analyzer configuration software.

> The base is shown with the values in binary.

APIC Bus Symbols

LABEL = Signals	Symbol	Value
ArbID = Valid, Cycle, ArbID	PIC 0	0 10 0000
	PIC 1	0 10 0001
	PIC 2	0 10 0010
	PIC 3	0 10 0011
	PIC 4	0 10 0100
	PIC 5	0 10 0101
	PIC 6	0 10 0110
	PIC 7	0 10 0111
	PIC 8	0 10 1000
	PIC 9	0 10 1001
	PIC 10	0 10 1010
	PIC 11	0 10 1011
	PIC 12	0 10 1100
	PIC 13	0 10 1101
	PIC 14	0 10 1110
	PIC 15	0 10 1111
Vector = Valid, Cycle, Vector	Vector 0h	0 10 00000000
	Vector 1h	0 10 00000001
	Vector 2h	0 10 00000010
	:	:
	Vector nh	0 10 n
	:	:
	Vector FFh	0 10 11111111

Error = Valid, Error, Cycle	Arbitration ID Idle Cycle Error Post Amble Error Priority Cycle Tie ID Ard Cycle unknown	1 001 01 1 010 01 1 011 01 1 100 01 1 110 01 1 111 01
EOI = Valid, EOI, Cycle	EOI Cycle Normal Cycle	0 1 10 0 0 10
C1Stat = Valid, C1Stat, Cycle	Checksum 3 Checksum 2 Checksum 1 Checksum 0	0 00 10 0 01 10 0 10 10 0 11 10
A Stat = Valid, A Stat, Delivery Mode, Cycle	CS OK, no foc CS OK, focus CS OK CS Error Error	0 00 001 10 0 10 001 10 0 00 xxx 10 0 11 xxx 10 0 01 xxx 10
A1Stat = Valid, EOI, A Stat, A1Stat, Delivery Mode, Cycle	Go for LP Arb End and Retry Retry Accept Error Accepted Error Bus Not Driven	0 0 00 11 001 10 (low priority) 0 0 00 10 001 10 (low priority) 0 1 00 11 000 10 0 1 00 0x xxx 10 0 x 00 10 xxx 10 0 0 1x x0 xxx 10 0 x xx xx xxx 10
DestMo = Valid, EOI, Destination Mode, Cycle	Logical Physical	0 0 1 10 0 0 0 10
Delive = Valid, EOI, Delivery Mode, Cycle	Fixed Lowest Priority SMI Remote Read NMI INIT Start Up reserved	0 0 000 10 0 0 001 10 0 0 010 10 0 0 011 10 0 0 100 10 0 0 101 10 0 0 110 10 0 0 111 10
Level = Valid, EOI, Level, Cycle	Assert De-assert	0 0 1 10 0 0 0 10

Trigge = Valid, EOI, Trigger, Cycle	Level Edge	0 0 1 10 0 0 0 10
Prior = Valid, Cycle, Prior	PIC 0 PIC 1 PIC 2 PIC 3 PIC 4 PIC 5 PIC 6 PIC 7 PIC 8 PIC 9 PIC 10 PIC 11 PIC 12 PIC 13 PIC 14 PIC 15	0 10 0000 0 10 0001 0 10 0010 0 10 0011 0 10 0100 0 10 0101 0 10 0110 0 10 0111 0 10 1000 0 10 1001 0 10 1010 0 10 1011 0 10 1100 0 10 1101 0 10 1110 0 10 1111

TieID = Valid, Delivery Mode, Cycle, TieID (two-pod) TieID = Valid, TieID, A Stat, A1Stat, Delivery Mode, Cycle (four-pod)		two-pod | four-pod
	PIC 0	0 001 01 0000 | 0 0000 00 11 001 10
	PIC 1	0 001 01 0001 | 0 0001 00 11 001 10
	PIC 2	0 001 01 0010 | 0 0010 00 11 001 10
	PIC 3	0 001 01 0011 | 0 0011 00 11 001 10
	PIC 4	0 001 01 0100 | 0 0100 00 11 001 10
	PIC 5	0 001 01 0101 | 0 0101 00 11 001 10
	PIC 6	0 001 01 0110 | 0 0110 00 11 001 10
	PIC 7	0 001 01 0111 | 0 0111 00 11 001 10
	PIC 8	0 001 01 1000 | 0 1000 00 11 001 10
	PIC 9	0 001 01 1001 | 0 1001 00 11 001 10
	PIC 10	0 001 01 1010 | 0 1010 00 11 001 10
	PIC 11	0 001 01 1011 | 0 1011 00 11 001 10
	PIC 12	0 001 01 1100 | 0 1100 00 11 001 10
	PIC 13	0 001 01 1101 | 0 1101 00 11 001 10
	PIC 14	0 001 01 1110 | 0 1110 00 11 001 10
	PIC 15	0 001 01 1111 | 0 1111 00 11 001 10
S Stat (data valid) = Valid, Cycle, S Stat (two-pod) S Stat (data valid) = Valid, S Stat, Delivery Mode, Cycle (four-pod)		two-pod | four-pod
	Valid	0 01 11 | 0 11 011 10
	Invalid	0 01 00 | 0 00 011 10
	Invalid	0 01 01 | 0 01 011 10
	Invalid	0 01 10 | 0 10 011 10
	----	x xx xx | x xx xxx xx
C2Stat = Valid, Cycle, C2Stat (two-pod) C2Stat = Valid, C2Stat, Delivery Mode, Cycle (four-pod)		two-pod | four-pod
	Checksum 0	0 01 00 | 0 00 011 10
	Checksum 1	0 01 01 | 0 01 011 10
	Checksum 2	0 01 10 | 0 10 011 10
	Checksum 3	0 01 11 | 0 11 011 10
	----	x xx xx | x xx xxx xx
A2Stat = Valid, A2Stat, Delivery Mode, Cycle (two-pod) A2Stat = Valid, A2Stat, A1Stat, Delivery Mode, Cycle (four-pod)		two-pod | four-pod
	Accept	0 10 001 01 | 0 10 00 011 01
	Error	0 11 001 01 | 0 11 00 011 01
	Error	0 0x 001 01 | 0 0x 00 011 01

DestID = Valid, Cycle, Destination ID (two-pod) DestID = Valid, Destination ID, Cycle (four-pod)	DestID 0h DestID 1h DestID 2h : DestID nh : DestID FFh	two-pod | four-pod 0 01 00000000 | 0 00000000 10 0 01 00000001 | 0 00000001 10 0 01 00000010 | 0 00000010 10 : | : 0 01 n | 0 n 10 : | : 0 01 11111111 | 0 11111111 10
UData = Valid, Data, Cycle (two-pod) UData = Valid, Data, Delive, Cycle four-pod)	---- ----	two-pod | four-pod 0 (16 data) 01 | 0 (16 data) xxx 10 x (16 data) xx | x (16 data) xxx xx
LData = Valid, Data, Cycle (two-pod) LData = Valid, Data, Delive, Cycle (four-pod)	---- ----	two-pod | four-pod 0 (16 data) 00 | 0 (16 data) xxx 10 x (16 data) xx | x (16 data) xxx xx

To display captured state data

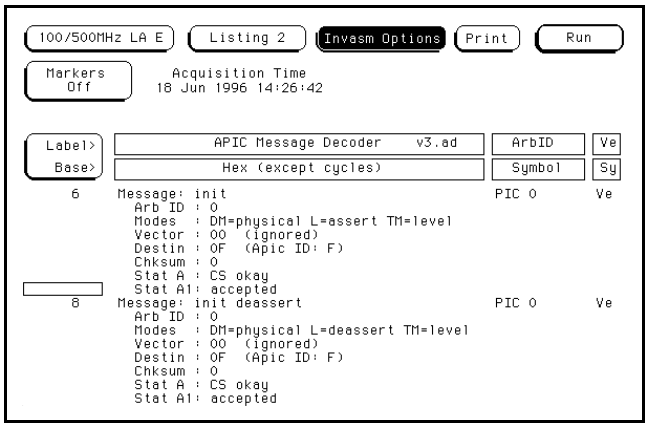
- **Select the Listing Menu for your logic analyzer.**

  The logic analyzer displays captured data in the Listing Menu. The inverse assembler processes the captured data in a transaction-based format.

  If your trace listing doesn't appear to be correct (capturing the same RAM address twice, for example), make sure the preprocessor interface hardware is configured for state analysis. The "Invasm Options" field will appear at the top of the Listing Menu screen when the logic analyzer is configured for state analysis. See Chapter 1 to review the hardware configuration, correct it if needed, and then run the trace again.

Example

The following figure shows the Listing Menu display for the HP 16550A logic analyzer using the two-pod inverse assembler.



Logic Analyzer Listing Menu

This section discusses the general output format of the inverse assembler, and any APIC-specific information you will need.

The APIC inverse assembler supports filter options based on Cycle number. You can Show or Suppress the second and third cycles.

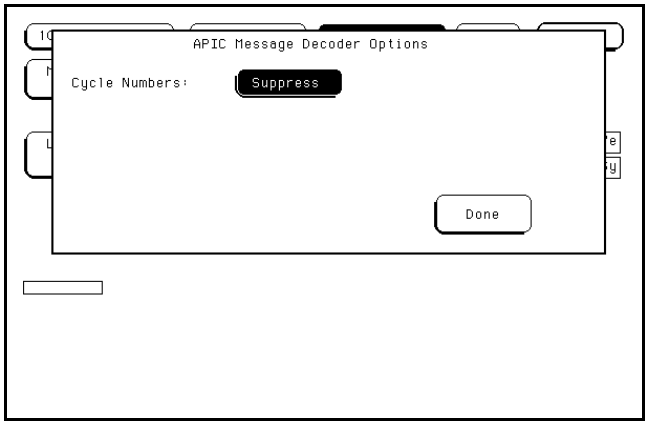
The next few paragraphs describe the general output format of the inverse assembler.

Numeric Format

For data, the numeric output from the inverse assembler is in hexadecimal format. All other numbers are in decimal format.

Show/Suppress

The Suppress/Show settings determine whether the second and third cycles are shown or suppressed on the logic analyzer display. The Show/Suppress settings do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined later with different settings, for different analysis requirements.



Filter Menu

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

Inverse Assembler Exception Messages

APIC bus messages do not have a way of uniquely identifying a message start. It is possible to start interpreting a message in the middle of a message stream with incorrect results. The preprocessor hardware attempts to track the APIC messages and look for patterns to uniquely identify an APIC message. When it doesn't see an expected pattern, it is flagged as an exception, the information captured to that point is sent to the logic analyzer, and the hardware begins looking for another possible message start.

Protocol violations

The preprocessor detects the following APIC Bus exceptions (defined as Error in symbol table):

Arbitration ID Cycle Defined as a logic high on D0 during arbitration ID cycles.

Idle Cycle defined as a logic high on D0 during the idle cycle.

Post Amble Cycle defined as a logic high on D0 during the post amble cycle.

Priority Cycle defined as a logic high on D0 during the priority ID cycles.

Tie ID Arb Cycle defined as a logic high on D0 during the lowest priority tie arbitration ID cycles.

When the preprocessor detects one of the above exception conditions, it aborts capturing the message and sends what information it had captured up to that point. The inverse assembler does not try to interpret the data, but only reports which exception was detected. The defined symbols can be used to interpret what was captured before the message; however, be aware that the exception occurred before the complete message was captured and may contain information from the last successfully captured APIC message.

The inverse assembler does not attempt to do a complete job of detecting protocol violations. Undetected protocol violations may cause the inverse assembler to display incorrect results.

To trigger on APIC message events, it is necessary to know which configuration, either 2 pod or 4 pod, the preprocessor is operating on. When used with a Pentium® or Pentium® Pro preprocessor interface, it is a two-pod configuration. The configuration determines on which cycle the APIC message information is sent, as shown in the following table:

Cycle	2 Pod	4 Pod
1	ArbID EOI Vector/register Dest Mode Level Trigger Delivery Mode Checksum A Status A1 Status Error	ArbID EOI Vector/register Dest Mode Level Trigger Delivery Mode Checksum A Status A1 Status Error Priority ID LP Arb Tie ID S Status Checksum 2 Status A2 Status Destination ID Upper Data word
2	Priority ID LP Arb Tie ID S Status Checksum 2 Status A2 Status Destination ID Upper Data word	Lower Data word
3	Lower Data Word	

The 16505A Protocol Analyzer configuration files have the above groups assigned to three of the patterns to simplify setting up triggering. The HP 16500B does not have the the same grouping capability and hence, has all of the labels associated with each trigger pattern.

To capture actual APIC Bus serial line signals

All messages sent by the APIC preprocessor are qualified by a high K clock. This is set up as the default mode in the format section. Using the K high qualifier to store messages ensures that the memory is filled with only APIC messages. The preprocessor also passes through the APIC serial signals on the first pod. To capture the serial bus events, the K high qualifier in the format section should be turned off. This will capture data on every APIC clock cycle, filling the data memory with everything, including the long gaps between APIC messages.

To trigger on Delivery Mode

The delivery mode message types are defined in the Delive symbol. Select the type of message type to trigger on under the Delive symbol and set the other symbols to 'don't cares' (usually defined as '----' under the symbol name). Set up the trigger menu sequencer level to "while storing anystate, trigger on "a", where "a" is the pattern defined in the first step.

To trigger on a particular vector

Vector addresses are defined in the Vector symbol. The symbol has definitions for all of the vectors. The setup is the same as for Delivery mode as defined above.

To trigger on multiple criterion

Triggering on multiple criterion is similar to the above with the caveat that one must pay attention to the configuration that is in use and how the criterion breaks out into cycles as shown in the above table. For example, to trigger on a Lowest Priority message type and a particular destination ID, the Delive symbol and the DestID symbol would be used. If a 4 pod configuration is being used, these two symbols could be combined into one pattern and the trigger sequence level would be set up as in the previous examples. However, if the 2 pod configuration is being used, the symbols would have to be assigned to two different patterns. The first trigger sequence level would be assigned to find the Delive symbol, and the second trigger sequence level would be assigned to find and trigger on the DestID symbol. Using the pre-defined patterns from the HP 16505A Protocol Analyzer simplifies setting up the patterns since the symbols are already grouped according to cycles.

To trigger on an APIC exception message

APIC exception messages are those defined in the section on Inverse Assembler exception Messages. To trigger on an exception message, use the symbols defined in the Error label.

To trigger on Data in Remote Read message

Remote read data is spread across multiple cycles in the preprocessor. To trigger on a particular data pattern, it will have to be broken into a trigger sequence. It will also be necessary to know whether two or four pods are being used, as this affects which cycle the data is on.

The data has been broken into upper and lower words, and labels have been defined to help with the setup. The labels are UData and LData, respectively.

In addition to the 16 bits for each word, there is also one bit for valid message and one bit for cycle number. In addition, the four-pod configuration also includes the three bits for delivery mode to help distinguish from random data.

It is informative to look at the Format setup to see how the bits are assigned in the label. Note that the signals are defined as inverted under the Format

setup to transform electrical values to logical values, as defined in the APIC sppecification.

A message is valid when the K clock is high. The cycle number for the two and four pod configuration is listed at the beginning of this section. Because of the inversion, the Valid bit and the Cycle bits also have to be inverted or the Format labels have to be changed to "+" to match how the data will be interpreted.

Example: Triggering on 0x12345678 using a four-pod configuration

Because the data is broken into upper and lower words, two symbols will have to be created and a trigger sequence used. The upper word, 0x1234, would occur on cycle 1 when the K clock is high. The lower word would appear on cycle 2 when the K clock is high. A remote read corresponds to logical 011.

Because cycle and K are active high, they become inverted in the UData and LData symbols. The symbols look like this:

UData (Valid, Data, Delive, Cycle) = 0 0001 0010 0011 0100 011 10
LData (Valid, Data, Delive, Cycle) = 0 0101 0110 0111 1000 011 01

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the HP2467A hardware including product, electrical, and environmental characteristics, signal mapping, a brief theory of operation, and repair information.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Product Characteristics	
Microprocessors Supported	Intel APIC Bus microprocessors. The HP E2467A can be used standalone for APIC bus analysis, or with Pentium® or Pentium® Pro preprocessor interfaces for APIC Bus and microprocessor analysis.
Package Supported	Any target system in which APIC Clk, D0, and D1 can be probed.
Accessories Supported	HP E2457A for Pentium® microprocessor and APIC Bus analysis, HP E2466A/B for Pentium® Pro microprocessor and APIC Bus analysis.
Logic Analyzer Required	HP 16500B mainframe with HP 16550A, HP 16554A, HP 16555A, or HP 16556A logic analyzer.
Number of Probes Used	Two or four 17-channel probes are required for inverse assembly.
Microprocessor Operations Displayed	Arbitration ID, Interrupt Vector, Error Number, EOI Status, Checksum, A Status, A1 Status, A2 Status, S Status, Destination Mode, Destination ID, Delivery Mode, Priority Arbitration ID, Level, and Trigger.
Additional Capabilities	When used with the HP E2457A or HP E2466A/B preprocessor interfaces, the APIC Bus preprocessor interface can be used to cross-trigger the logic analyzer on APIC Bus cycles.
Timing Analysis	None.
Electrical Characteristics	
Power Requirements	500 mA at +5VDC, supplied by the logic analyzer.
Signal Line Loading	The HP E2467A Preprocessor Interface adds 100 KOhms and 8 pF to APIC Clk, D0, and D1.
Maximum Clock Speed	33 MHz Clock Input.

Environmental Characteristics

Temperature	Operating	0 to + 55 degrees C +32 to +131 degrees F
	Nonoperating	-40 to + 75 degrees C -40 to +167 degrees F
Altitude	Operating	4,600 m (15,000 feet)
	Nonoperating	15,3000 m (50,000 feet)
Humidity	Up to 90% noncondensing. Avoid sudden , extreme temperature changes which could cause condensation on the circuit board.	

Theory of Operation and Clocking

The HP E2467A APIC Bus preprocessor captures the APIC serial messages and sends them to the logic analyzer in parallel to simplify triggering. It operates in either a 2-pod or a 4-pod configuration. It watches the bus, looking for a start of message as indicated by the PIC D0 signal going high (electrically low). It then tracks the signals, looking for expected patterns. After it has captured an entire message or detected an error condition, it sends the message up to the logic analyzer.

Messages sent to the logic analyzer are qualified with the K clock.When the K clock is high, the message is valid. Most messages will take more than one clock cycle to send the message to the logic analyzer. Therefore, the cycle number has been encoded on two bits on one of the pods.

The APIC serial line signals are passed through the HP E2467A preprocessor up to the logic analyzer. The APIC Clock is used as the master clock while the D1 and D0 signals appear on Pod One as signals 1 and 0, respectively.

All three signals (clock, D1, and D0) are buffered through the preprocessor.

Signal-to-Connector Mapping

The following table shows the electrical interconnections implemented with the preprocessor interface. Note that the signals to the logic analyzer are different for two-pod and four-pod logic analyzers, and that they depend on the cycle.

Two-Pod Logic Analyzer Signal List

Pod	2x20 pin	Analyzer Bit	APIC Signal	Analyzer Labels Cycle 1	Analyzer Labels Cycle 2	Analyzer Labels Cycle 3
P1	3	CLK1		PICCLK	PICCLK	
P1	7	D15		cycle	cycle	cycle
P1	9	D14		cycle	cycle	cycle
P1	11	D13		ArbID	DestID	
P1	13	D12		ArbID	DestID	
P1	15	D11		ArbID	DestID	
P1	17	D10		ArbID	DestID	
P1	19	D9		Vector	DestID	
P1	21	D8		Vector	DestID	
P1	23	D7		Vector	DestID	
P1	25	D6		Vector	DestID	
P1	27	D5		Vector	S Stat/TieID	
P1	29	D4		Vector	S Stat/TieID	
P1	31	D3		Vector	C2Stat/TieID	
P1	33	D2		Vector	C2Stat/TieID	
P1	35	D1	D1	PICD1	PICD1	
P1	37	D0	D0	PICD0	PICD0	

Two-Pod Logic Analyzer Signal List

Pod	2x20 pin	Analyzer Bit	APIC Signal	Analyzer Labels Cycle 1	Analyzer Labels Cycle 2	Analyzer Labels Cycle 3
P2	3	CLK1		VALID	VALID	VALID
P2	7	D15		error	UData/Prior	LData
P2	9	D14		error	UData/Prior	LData
P2	11	D13		error	UData/Prior	LData
P2	13	D12		EOI	UData/Prior	LData
P2	15	D11		C1 Stat	UData/Prior	LData
P2	17	D10		C1 Stat	UData/Prior	LData
P2	19	D9		A Stat	UData/Prior	LData
P2	21	D8		A Stat	UData/Prior	LData
P2	23	D7		A1Stat	UData/A2Stat	LData
P2	25	D6		A1Stat	UData/A2Stat	LData
P2	27	D5		DestMo	UData	LData
P2	29	D4		Delive	UData	LData
P2	31	D3		Delive	UData	LData
P2	33	D2		Delive	UData	LData
P2	35	D1		Level	UData	LData
P2	37	D0		Trigge	UData	LData

Two-Pod Logic Analyzer Signal List

Four-Pod Logic Analyzer Signal List

Pod	2x20 pin	Analyzer Bit	APIC Signal	Analyzer Labels Cycle 1	Analyzer Labels Cycle 2
P1	3	CLK1		PICCLK	PICCLK
P1	7	D15		cycle	cycle
P1	9	D14		cycle	cycle
P1	11	D13		ArbID	
P1	13	D12		ArbID	
P1	15	D11		ArbID	
P1	17	D10		ArbID	
P1	19	D9		Vector	
P1	21	D8		Vector	
P1	23	D7		Vector	
P1	25	D6		Vector	
P1	27	D5		Vector	
P1	29	D4		Vector	
P1	31	D3		Vector	
P1	33	D2		Vector	
P1	35	D1	D1	PICD1	
P1	37	D0	D0	PICD0	

Four-Pod Logic Analyzer Signal List

Pod	2x20 pin	Analyzer Bit	APIC Signal	Analyzer Labels Cycle 1	Analyzer Labels Cycle 2
P2	3	CLK1		VALID	VALID
P2	7	D15		error	
P2	9	D14		error	
P2	11	D13		error	
P2	13	D12		EOI	
P2	15	D11		C1 Stat	
P2	17	D10		C1 Stat	
P2	19	D9		A Stat	
P2	21	D8		A Stat	
P2	23	D7		A1Stat	
P2	25	D6		A1Stat	
P2	27	D5		DestMo	
P2	29	D4		Delive	
P2	31	D3		Delive	
P2	33	D2		Delive	
P2	35	D1		Level	
P2	37	D0		Trigge	

Four-Pod Logic Analyzer Signal List

Pod	2x20 pin	Analyzer Bit	APIC Signal	Analyzer Labels Cycle 1	Analyzer Labels Cycle 2
P3	3	CLK1			
P3	7	D15			
P3	9	D14			
P3	11	D13		DestID	
P3	13	D12		DestID	
P3	15	D11		DestID	
P3	17	D10		DestID	
P3	19	D9		DestID	
P3	21	D8		DestID	
P3	23	D7		DestID	
P3	25	D6		DestID	
P3	27	D5		S Stat/TieID	
P3	29	D4		S Stat/TieID	
P3	31	D3		C2Stat/TieID	
P3	33	D2		C2Stat/TieID	
P3	35	D1			
P3	37	D0			

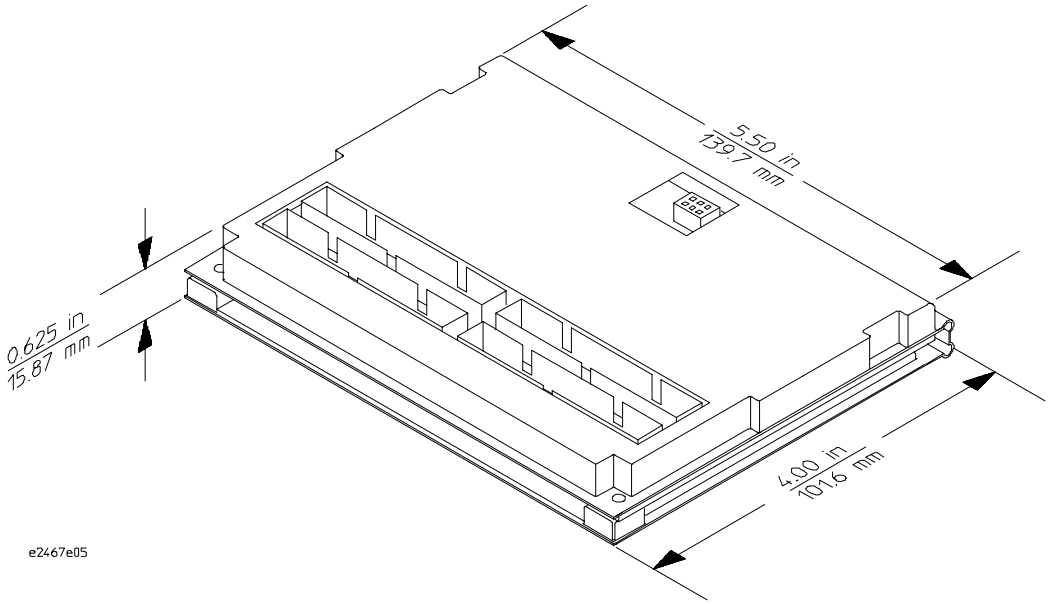
Four-Pod Logic Analyzer Signal List

Pod	2x20 pin	Analyzer Bit	APIC Signal	Analyzer Labels Cycle 1	Analyzer Labels Cycle 2
P4	3	CLK1			
P4	7	D15		UData/Prior	LData
P4	9	D14		UData/Prior	LData
P4	11	D13		UData/Prior	LData
P4	13	D12		UData/Prior	LData
P4	15	D11		UData/Prior	LData
P4	17	D10		UData/Prior	LData
P4	19	D9		UData/Prior	LData
P4	21	D8		UData/Prior	LData
P4	23	D7		UData/A2Stat	LData
P4	25	D6		UData/A2Stat	LData
P4	27	D5		UData	LData
P4	29	D4		UData	LData
P4	31	D3		UData	LData
P4	33	D2		UData	LData
P4	35	D1	D1	UData	LData
P4	37	D0	D0	UData	LData

Four-Pod Logic Analyzer Signal List

Circuit Board Dimensions

The following figure gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.



Dimensions

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Replaceable Parts

HP Part Number	Description
E2467-69501	Circuit board assembly
E2467-68700	Inverse assembler disk pouch
5090-4355	Grabbers (Qty 20)
5959-9334	2" probe grounds (Qty 5)
E2467-82101	Probe Lead

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the preprocessor interface or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See “Capacitive Loading” in this chapter for information on other sources of intermittent data errors.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Preprocessor Problems

This section lists problems that you might encounter when using a preprocessor. If the solutions suggested here do not correct the problem, you may have a damaged preprocessor. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the preprocessor interface, the microprocessor (if socketed) or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the preprocessor and target system.**

  1 Power up the analyzer and preprocessor.

  2 Power up the target system.

  If you power up the target system before you power up the preprocessor, interface circuitry in the preprocessor may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the preprocessor interface are properly rotated and aligned, so that the index pin on the microprocessor (such as pin 1 or A1) matches the index pin on the preprocessor interface.**

- ☐ **Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and are firmly inserted.**

- ☐ **Reduce the number of extender sockets.**

See Also “Capacitive Loading” in this appendix.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- **Do a full reset of the target system before beginning the measurement.**

  Some preprocessor designs require a full reset to ensure correct configuration.

- **Ensure that your target system meets the timing requirements of the processor with the preprocessor probe installed.**

  See “Capacitive Loading” in this chapter. While preprocessor loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- **Ensure that you have sufficient cooling for the microprocessor.**

  Microprocessors such as the i486, Pentium®, and MC68040 generate substantial heat. This is exacerbated by the active circuitry on the preprocessor board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the preprocessor interface, or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- **Remove as many pin protectors, extenders, and adapters as possible.**

- **If multiple preprocessor interface solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct preprocessor connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and preprocessor cable numbers. Preprocessors must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each preprocessor are often altered to support that need. Thus, one preprocessor might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 1 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some preprocessors also require other data labels. See Chapter 2 for more information.

- ☐ Verify that storage qualification has not excluded storage of all the needed message cycle numbers.

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ Ensure that the inverse assembler is on the same disk as the configuration files you are loading.

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler or rename it, the configuration process will fail to load the disassembler.

  See Chapter 1 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and not always be related to the event you are trying to capture with the oscilloscope.

Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted, and that it is located in the same directory as the configuration file.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ **Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.**

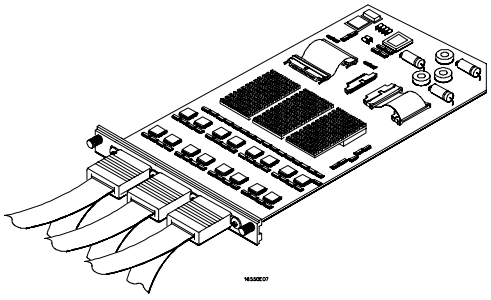
See Also Chapter 1 describes how to load configuration files.

"Selected File is Incompatible"

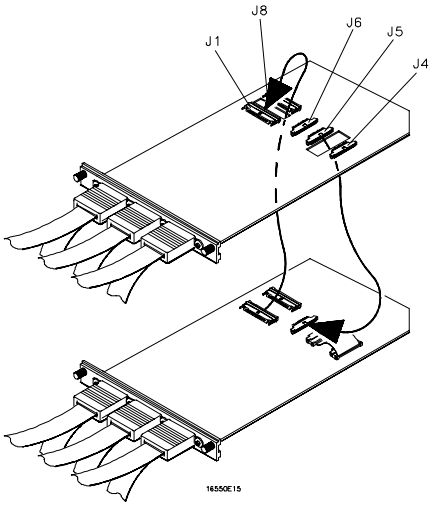
This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly for one or two HP 16550A logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16550A Installations



Cable Connections for Two-Card HP 16550A Installations

See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

"Slow or Missing Clock"

- This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.
- This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See Chapter 1 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allows it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Restricted Rights Legend

Use, duplication, or disclosure by the U.S. Government is subject to restrictions set forth in subparagraph (C) (1) (ii) of the Rights in Technical Data and Computer Software Clause in DFARS 252.227-7013.
Hewlett-Packard Company, 3000 Hanover Street, Palo Alto, CA 94304 U.S.A.
Rights for non-DOD U.S. Government Departments and Agencies are set forth in FAR 52.227-19(c)(1,2).

Document Warranty

The information contained in this document is subject to change without notice.

Hewlett-Packard makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability or fitness for a particular purpose.

Hewlett-Packard shall not be liable for errors contained herein or for damages in connection with the furnishing, performance, or use of this material.

Safety

This apparatus has been designed and tested in according to Internationaol Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded. In addition, note the external markings on the product that are described under "Safety Symbols."

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

Hewlett-Packard
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument software, or firmware will be uninterrupted or error free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. Hewlett-Packard specifically disclaims the implied warranties of merchantability or fitness for a particular purpose.

Exclusive Remedies

The remedies provided herein are the buyer's sole and exclusive remedies. Hewlett-Packard shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales Office.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

About this edition

This is the *HP E2467A Intel APIC Bus Preprocessor Inteface User's Guide.*

Publication number
E2467-97002, January 1997
Printed in USA.

Print history is as follows:

E2467-97000, June 1996

E2467-97001, August 1996

New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.